CLAIMS

1. A Circuit for measuring the cell post voltage and internal impedance voltage in storage battery cells, comprising:
High Input Common Mode Voltage Differential Amplifier (1) and;
Reference Constant Voltage Circuit (2) and;
Direct Current Filter Circuit (3) and;
Buffer Circuit (4) and;
Direct Current Coupling Circuit (6) and;
Band Pass Filter (7) and;
Operational Amplifier Group (8) and;
A/D converter (5, 9) and CPU (10).

2. The circuit as claimed in Claim 1, wherein A/D converter (5, 9) and CPU (10) are replaced by A/D converter consisting of Multiplexer (MUX) circuit with a number of input channels and ADC circuit, and CPU (10)

3. The circuit as claimed in Claim 1, wherein A/D converter (5, 9) and CPU (10) are replaced by A/D converter and CPU built in a micro controller unit (MCU) of commercialized devices.

4. The circuit as claimed in Claim 2, wherein the cell post voltage (V_{dc}) which is buffered and outputted by the Buffer (4), the impedance voltage signal (V_{ls}') which is amplified in a number of stages and outputted with a number of signals by Operational amplifier group (8), and the analog signals of ±10V range like constant current signal (Is) are respectively inputted to the each input channel of the multiplexer (MUX) circuit and;
the above analog signals selected by the Select signal of the CPU (10) are inputted into the ADC circuit of the 12 Bit A/D converter (9a).

5. The Circuit as claimed in Claim 1 or 3, wherein the output voltage obtained in the above Differential Amplifier (1) is divided as one third at the Divider/Buffer, and the above Operational amplifier group (8) is composed of a number of amplifiers whose amplification gain is different and Adders connected to the back terminals of the above amplifiers respectively.

6. The circuit as claimed in Claim 1, wherein Band pass filter (7) in which the narrow-band pass filters which consist of two condensers, three resistors and one Operational amplifier, are comprised in a two-stage dependent connection.

7. A Circuit for measuring the cell post voltage and internal impedance voltage in storage battery cells, comprising:

(i) the outputs of the sense terminals (③,④) are connected to the none-inverting and inverting input terminals of a high input common mode voltage differential amplifier(1),

the negative (-) constant voltage (Vref) which is generated by the Reference Constant Voltage Circuit (2) is inputted (connected) into the offset terminal of the above differential amplifier(1),

the output of the above differential amplifier(1) is filtered in the disclosed direct current filter circuit (3) and then buffered in the Buffer (4),

and converted from analog to digital;

(ii) and on the hand, the output of the above differential amplifier(1) is passed through Direct Current Coupling Circuit (6) and then transformed to the alternating signal of impedance voltage (V_{ls}'),

and the above alternating signal is passed through band pass filter(7) and Operational amplifier group (8),

and then converted from analog to digital.

8. The circuit as claimed in Claim 7, wherein the Reference Constant Voltage Circuit (2) has two constant voltage diodes, ZD2 and ZD3 and the current limiting resistor R3 in a serial connection and,

the negative (-) constant voltage generated by the above Reference Constant Voltage Circuit (2) is connected to the offset terminal of the differential amplifier (1) through the buffer circuit and,

the diode D1, variable resistor R4 and diode D2 are serially connected on the each terminal of the above constant voltage diode ZD2,

and the central terminal of the above variable resistor R4 connected to the ADJ terminal of the above constant voltage diode ZD2 to make it possible to minutely adjust the offset reference voltage (Vref) as the variable resistor R4.

9. The circuit as claimed in Claim 7, wherein the offset terminal of the above differential amplifier(1) is connected with the negative (-) constant voltage of –8V which is generated by the disclosed Reference Constant Voltage Circuit (2).

10. The circuit as claimed in Claim 7, wherein High Input Common Mode Voltage Differential Amplifier (1) comprises the differential Operational amplifier element whose input impedance is very high and the hundreds of kilo ohm (KΩ) resistors connected to the inverting and none-inverting input circuits of the above differential Operational amplifier element and;

the disclosed Reference Constant Voltage Circuit (2) is connected to the offset adjustment terminal of the above differential Operational amplifier element.